IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application for:

METHOD AND APPARATUS FOR REDUCING CHARGE INJECTION IN A FET SWITCH

Inventors: Sylvia Jane Budak
2053 Ridge West Drive
Windsor, Colorado 80550

Christopher Judd Kemp
645 Bear Trap Way
Monument, Colorado 80132

Docket Number: 10031023-1

METHOD AND APPARATUS FOR REDUCING CHARGE INJECTION IN A FET SWITCH

FIELD OF THE INVENTION

This invention relates generally to the field of electrical switching. More particularly, this invention relates to a method and apparatus for reducing charge injection in a Field-Effect Transistor (FET) switch.

BACKGROUND

Field-Effect Transistor (FET) switches often introduce undesired voltage transients. For example, an N-channel, enhancement mode, Metal-oxide Semiconductor Field-Effect Transistor (MOSFET) switch is turned on by applying a gate drive signal to the gate of the FET. The gate drive signal makes a voltage transition from a supply level to a level above the analog signal to be switched. When the FET switch turns off, the opposite transition is made. In either case, part of the drive signal transition occurs while the switch FET is on, and part while the switch FET is off. For the 'off' part of the transition, the gate-to-drain capacitance of the FET couples into the input node and injects charge into the input, causing a voltage transient. On the other hand, for the 'on' part of the drive signal transition, the sum of the gate-to-drain, gate-to-source and gate-to-channel capacitances of the FET couples into the input node and injects charge into the input, causing a voltage transient.

One approach to reducing or eliminating the charge injection is to use a compensating FET and a capacitor. In this approach, the gate drive voltage of the compensation FET and/or capacitor is equal in magnitude to that of the switch FET but opposite in direction. The length of time the FETs are on varies with the input signal level and therefore changes the total amount of charge transfer. Consequently, this compensation technique will be less effective for some voltages than others. Another approach uses a programmable digital-to-analog converter (DAC) in an auto-calibration loop. A zero voltage level is applied to the high impedance input of the DAC. Measurements are then made using the analog-to-digital converter (ADC) of a digital multi-meter while the switch is toggled on and off. A programmable capacitor is adjusted until the reading is zero. This technique is expensive, due to external components, and requires a calibration algorithm. Additionally, the speed of compensation is limited, so high frequency injection is not well compensated.

OVERVIEW OF CERTAIN EMBODIMENTS

The present invention relates generally to the compensation of charge injection in FET switches. Objects and features of the invention will become apparent to those of ordinary skill in the art upon consideration of the following detailed description of the invention.

In one embodiment of the invention a switch includes a switch FET and two compensating FETs coupled to an input node. Gate drive signals for the two compensating FETs are generated by a gate drive circuit dependent upon the analog input signal and gate drive signal to the switch FET.

BRIEF DESCRIPTION OF THE DRAWINGS

The novel features believed characteristic of the invention are set forth in the appended claims. The invention itself, however, as well as the preferred mode of use, and further objects and advantages thereof, will best be understood by reference to the following detailed description of an illustrative embodiment when read in conjunction with the accompanying drawing(s), wherein:

FIG. 1 is a schematic diagram of a charge compensation circuit in accordance with certain embodiments of the invention.

FIG. 2 is a diagram depicting a switch FET gate drive signal in a charge compensation circuit in accordance with certain embodiments of the invention.

FIG. 3 is a diagram depicting further gate drive signals in a charge compensation circuit in accordance with certain embodiments of the invention.

FIG. 4 is a timing diagram depicting logic signals in a charge compensation circuit in accordance with certain embodiments of the invention.

FIG. 5 is a schematic diagram of a gate-drive circuit in accordance with certain embodiments of the invention.

FIG. 6 is a graph showing reduction of charge injection by use of a charge compensation circuit.

DETAILEDDESCRIPTION

While this invention is susceptible of embodiment in many different forms, there is shown in the drawings and will herein be described in detail one or more specific embodiments, with the understanding that the present disclosure is to be

considered as exemplary of the principles of the invention and not intended to limit the invention to the specific embodiments shown and described. In the description below, like reference numerals are used to describe the same, similar or corresponding parts in the several views of the drawings.

FIG. 1 is a simplified schematic diagram of FET switch 100 incorporating an exemplary charge compensation circuit. Referring to **FIG. 1**, the signal to be switched is applied to input node 102 and denoted as *Vin*. The switch 100 employs two separate compensation circuits that act as "dummy capacitors" and are used to minimize charge injection into the input node 102. In this embodiment, the first compensation circuit or dummy capacitor comprises a FET 104. The drive for the first dummy capacitor is provided on the line 106 by a gate drive circuit 150 described below with reference to **FIG. 5**. Referring to **FIG. 1**, the gate drive signal for FET 104 is denoted by *gatexlo*. The drain of the FET 104 is coupled to the input node 102. The FET 108 provides the second dummy capacitor. The drain, channel and source of the FET 108 are all coupled to the input node 102. The drive for the FET 108 is provided on the line 110 by the gate driver circuit 150. The gate drive signal for FET 108 is denoted by *gatexhi*. An optional capacitor 112, which may be a poly/metal1/metal2 capacitor of variable capacitance, for example, is included to allow for 'fine tuning' of the capacitance provided by the dummy capacitors. The switching function itself is provided by the FET 114. The gate drive for the FET 114 is provided by the gate drive signal 116, and is denoted by the signal *m1gate*. The '*x*' designation in the signals *gatexhi* and *gatexlo* signifies that these signals move opposite to the gate drive signal *m1gate* of the switch FET 114. That is, when the

signal *m1gate* is rising, the signals *gatexhi* and *gatexlo* are falling and vice versa. The '*hi*' and '*lo*' designations indicate the part of the *m1gate* signal transition for which the *gatexhi* and *gatexlo* signals are being used to balance the charge injection, as will be explained below. Capacitors 120 and 122 represent stray capacitance and circuit capacitance on the *Vin* node 102 and *Vout* node 118, respectively.

In one embodiment, the FETs 104, 108 and 114 are of the same design to allow for accurate capacitance matching and tracking. The FETs may be Metal-Oxide Semiconductor Field-Effect Transistors (MOSFETs) or Junction Field-Effect Transistors (JFETs), or similar gate-controlled devices.

It will be apparent to those of ordinary skill in the art, that any of the FETs 104, 108 and 114 may, in practice, be an assembly of devices constituting a switch. For example, the FET may be a pair of back-to-back DMOS devices, a pair of MOSFET devices, or a CMOS device made of an NMOS device in parallel with a PMOS device. In the sequel the term "FET" will be taken to include a combination of devices forming a switch.

The operation of the circuit in **FIG. 1** is now described for an exemplary embodiment. When the switch FET 114 turns on, the signal *m1gate* makes a voltage transition from a negative supply level *VSS2* to approximately 10V above the analog signal to be switched (*Vin*). The switch is turned on when the gate signal is at a switching voltage level $Vs=Vin + Vth$, where *Vth* is a threshold voltage level. When the switch FET 114 turns off, the opposite transition is made. In either case, part of the *m1gate* transition occurs while the switch FET is on, and part while the switch FET is off. For the 'off' part of the transition, only the gate-to-drain capacitance of

the FET 114 couples into the input node *Vin* and causes a voltage transient. On the other hand, for the 'on' part of the *m1gate* transition, the sum of the gate-to-drain, gate-to-source and gate-to-channel capacitances of the FET 114 couples gate voltage changes into the input node *Vin* and causes a voltage transient. If a single charge balancing capacitor is used, and it is driven between the same voltages as *m1gate* (but in the opposite direction), optimal charge injection compensation will occur only for one value of the input signal level. However, good performance is achieved over the entire range of input signal levels if charge injection compensation is performed separately for the two distinct parts of the *m1gate* voltage transition.

In the switch circuit, the dummy capacitance driven by the signal *gatexlo* compensates for the switch FET charge injection for the 'off' part of the *m1gate* signal transition, whereas the dummy capacitance driven by the signal *gatexhi* compensates for the switch FET charge injection for the 'on' part of the *m1gate* signal transition. As the signal *m1gate* rises (switch turning on), the *gatexlo* falls from the switching level *Vs* to the level *VSS2*, and *gatexhi* falls from the turn-on level (*Vbias* volts above the switching level, or approximately 10V above the input signal level) to the switching level. This equalizes the compensation charge, and the charge injected by the switch FET, for all levels of the input signal.

The gate control signals *gatexlo*, *gatexhi* and *m1gate* are generated by gate drive circuit 150. The drive circuit 150 receives the analog input signal *Vin* at input 152, a digital (logic) switching signal *m1* at input 154, and voltage supply signals *VSS1* and *VSS2* at input 156 and 158, respectively. An exemplary embodiment of the gate drive circuit 150 is described below with reference to **FIG. 5**.

The *gatexlo* and *gatexhi* signals, in addition to transitioning between the correct voltage levels, are also timed correctly to properly balance the injected charge. The relative timing of the signals is shown in **FIG. 2** and **FIG. 3**. The figures show the voltage V of the gate drive signals as a function of time, t when the switch is turned on and off. Referring to **FIG. 2**, the switch turn-on is initiated at time t_1 when the digital signal *m1* (154 in **FIG. 1**) goes high. The *m1gate* signal 204 that controls the switch FET begins to ramp upwards. At time t_2 the *m1gate* signal 204 rises to the level 202 of the switching voltage, $Vs=Vin+Vth$, such that the voltage *Vgs* from the FET gate to its source is equal to *Vth* and the device just turns on. The switch turn-off is initiated at time t_3 when the digital signal *m1* (154 in **FIG. 1**) goes low. The *m1gate* signal 204 begins to ramp downwards. At time t_4 the *m1gate* signal 204 falls below the level 202 of the switching voltage *Vs*, such that $Vgs<Vth$ and the device turns off.

Corresponding *gatexlo* and *gatexhi* signals are shown in **FIG. 3**. The gate driver circuit is designed such that, when the *m1gate* signal starts to rise at time t_1, the *gatexlo* signal 304 falls immediately, as shown in **FIG. 3,** but the *gatexhi* signal 302 does not fall until *m1gate* is above the switching voltage level at time t_2. When the *m1gate* signal starts to fall at time t_3, the *gatexhi* signal 302 rises immediately to a maximum level *Vbias* volts above the switching level *Vs*, but the *gatexlo* 304 does not rise until *m1gate* is below the switching voltage level at time t_4.

In one embodiment, the FETs are of the same type. In this embodiment the gate drive signals are given by:

$$gatexhi = Vs + Vbias + c1.(Vs - m1gate)$$

$$gatexlo = (1 - c1).(Vs - m1gate) + VSS2$$

where

$$c1 = \begin{cases} 1 & \text{if } m1gate > Vs \\ 0 & \text{otherwise} \end{cases}.$$

The net voltage change of *gatexhi*, *gatexlo* and *m1gate* is zero and so the net charge injection will be zero.

A signal indicating if the *m1gate* signal is above or below the switching level *Vs* may be obtained by passing the *m1gate* signal and a signal at the switching voltage level to a comparator. The output of the comparator is denoted by the logic signal *c1*. **FIG. 4** is a timing diagram showing the comparator output *c1* and a digital (logic) switch signal *m1* used to activate the FET switch. The assertion of the digital switch signal *m1* at t_1 (a signal is asserted when it takes the logic value 'true', which is the value 1 for positive logic, and is de-asserted when it takes the value 'false') causes the *m1gate* signal to start rising. The de-assertion of the digital switch signal *m1* at t_3 causes the *m1gate* signal to start falling. The comparator output *c1* is asserted when the *m1gate* signal is greater than the switching voltage level. The *gatexhi* signal should be falling, or at its minimum, during the time period $t_2<t<t_3$ i.e. the period when both *m1* and *c1* are asserted. The signal denoted as *h* is asserted during this period. The *gatexlo* signal should be falling, or at its minimum, during the time period $t_1<t<t_4$ i.e. the period when either *m1* or *c1* is asserted. The signal denoted as *l* is asserted during this period. In the gate drive circuit, the signals *h* and *l* may be obtained using simple logic circuits and using control voltage levels.

A truth table showing operation of the corresponding logic circuit is given in **Table 1**. The inputs to the logic circuit are the digital switching signal, *m1*, and the output of the comparator, *c1*. Starting from the 'off' position, the signal *l* is asserted first and de-asserted last.

5

Table 1.

Condition	*m1*	*c1*	*l* *m1* OR *c1*	*h* *m1* AND *c1*
switch off	0	0	0	0
initial turn-on	1	0	1	0
switch on	1	1	1	1
initial turn-off	0	1	1	0
switch off	0	0	0	0

FIG. 5 is a schematic diagram of an exemplary gate driver circuit 150 used to generate the gate drive signals *m1gate, gatexhi* and *gatexlo.* The analog input signal *Vin* enters at input 152. A level shifter 504 provides a voltage level at node 506 that is approximately 9V above the analog input signal level *Vin.* The analog input signal 152 is also coupled to unity gain buffer 508 to provide a buffered version of the analog input signal at node 510. An always-on current source 512 establishes a voltage at node 514, which is one diode drop above the analog input signal level. Another always-on current source 516, of equal value, establishes a voltage at node 518, which is one diode drop below the analog input signal level. The digital *m1* signal 154 controls the operation of current sources 522 and 524. When the digital *m1* signal is high, the *m1* current supply 522 is enabled and the *m1bar* current supply 524 is disabled. When the digital *m1* signal is low, the *m1* current supply 522 is disabled and the *m1bar* current supply 524 is enabled. Prior to the switch FET coming on, the digital *m1* signal 154 is low, hence the *m1gate* signal 116 is pulled to the bottom rail *VSS2* by the *m1bar* current source 524 and the *m1* current source 522 is off. In one

embodiment of the gate drive circuit 150, the current sources shown in **FIG. 5** are provided by the output of FET current mirrors, and so behave like simple resistor pullups/pulldowns when the voltage across them falls below the level required to keep the output FET in saturation. The output signal *l* of the OR gate 528 controls the current sources 530, 532 and 534. When *l* is high the source 530 is on; when *l* is low the current sources 532 and 534 are on. With *m1* low and *c1* low, the signal *l* is low. Hence the *l* current source 530 is off and the *lbar* current sources 532 and 534 are on. This establishes the analog signal level *Vin+Vth* at the *gatexlo* output 106. The output signal *h* of the AND gate 536 controls the current sources 540, 542 and 544. When *h* is high the sources 540 and 542 are on, when *h* is low the current source 544 is on. Hence, with *m1* low, the output signal *h* of the AND gate 536 is also low. The *h* current sources 540 and 542 are off and the *hbar* current source 544 is on. This establishes a voltage level of *Vs* plus 9V plus one diode drop on (i.e. the static turn-on level) on the *gatexhi* output 110.

A switch turn-on is initiated by the *m1* digital signal 154 going high. This turns off the *m1bar* current source 524 and turns on the *m1* current source 522, causing the *m1gate* signal 116 to ramp upward from the voltage level *VSS2*. The output *l* of the OR gate 528 goes high, turning on the *l* current source 530 and turning off the *lbar* current sources 532 and 534. This causes the *gatexlo* signal 106 to ramp downwards from the switching level *Vs* to the negative supply level *VSS2*. The output signal *h* of the AND gate 536 stays low until the level of the *m1gate* signal 116 exceeds the switching level *Vs*, at which time the output from comparator 548 switches. The signal *h* goes high, turning on the *h* current sources 540 and 542 and

turning off the *hbar* current source 544. This causes the *gatexhi* signal 110 to ramp downwards from the turn-on level to the switching level *Vs* as the *m1gate* signal continues to ramp positively to the static turn-on level.

A switch turn-off is initiated by the *m1* digital signal 154 going low. This turns on the *m1bar* current source 524 and turns off the *m1* current source 522, causing the *m1gate* signal 116 to ramp downwards from the static turn-on level. The output signal *h* of the AND gate 536 goes low turning off the *h* current sources 540 and 542 and turning on the *hbar* current source 544. This causes the *gatexhi* signal 110 to ramp upwards from the switching voltage level *Vs=Vin+Vth* to the static turn-on level. The output *l* of the OR gate 528 stays high until the level of the *m1gate* signal 116 falls below the switching voltage level, at which time the output from comparator 548 switches. In one embodiment of the invention, this is achieved by setting a threshold of *Vth* in the comparator, so that the comparator switches when *m1gate=Vin+Vth*. The signal *l* then goes low, turning-off the *l* current source 530 and turning on the *lbar* current sources 532 and 534. This causes the *gatexlo* signal 106 to ramp upward from the negative supply level *VSS2* to the switching voltage level as the signal *m1gate* continues to ramp negatively to *VSS2*.

The diodes 560 in **FIG. 5** are used to block current flow in particular states of the circuit and to set voltage levels.

In an alternative embodiment of the gate drive circuit 150, the comparator 548 switches when *m1gate=Vin*. In this embodiment, the capacitor 112 in Figure 1 can be used to correct for the error introduced by neglecting the threshold voltage *Vth* of

the switching FET. This approach works well when the threshold voltage *Vth* is constant over the entire input signal range.

FIG. 6 shows two graphs of "voltage transients" caused by charge injection in an N-channel enhancement mode MOSFET switch. The voltage is plotted as function of time. The upper graph shows the voltage due to charge injection without compensation. The peak voltage is approximately 25 mV. The lower graph shows the voltage when a charge compensation circuit is employed. The peak voltage is less than 1 mV.

Those of ordinary skill in the art will recognize that the present invention has been described in terms of exemplary embodiments based upon use of MOSFET devices, current sources and logic circuits. However, the invention should not be so limited, since the present invention could be implemented using hardware component equivalents.

While the invention has been described in conjunction with specific embodiments, it is evident that many alternatives, modifications, permutations and variations will become apparent to those of ordinary skill in the art in light of the foregoing description. Accordingly, it is intended that the present invention embrace all such alternatives, modifications and variations as fall within the scope of the appended claims.

What is claimed is: